Detector Technology Development for NGST

Craig McCreight
NASA Ames

(650) 604-6549
cmccreight@mail.arc.nasa.gov

Objectives

- Develop multiple technology options which meet NGST requirements; in near-IR and thermal-IR

- Follow strategies outlined in NGST Detector Development Plan, and at Origins Technology Workshop

- Incorporate prior low-background art & science (e.g., SIRTF), while also looking for new, emerging technologies

- Carefully characterize and demonstrate technologies (lab, telescope, space?)

- Involve science community in development and demonstration phases

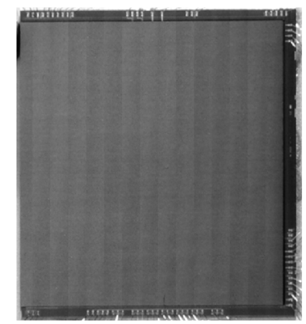
NGST Performance Goals

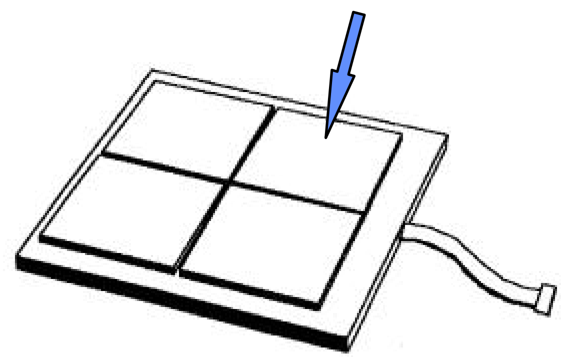
	Near-IR		Thermal-IR	
	Goal	Stretch	Goal	Stretch
Wavelength Range (µm)	1 – 5		5 and longward – at least to 10. 20 + desirable	
Operating Temperature (K)	30		30?? or as high as possible	TBD
Largest Format	4 ea. 4 k x 4 k		1 k x 1 k	
Individual Array Format	1 k x 1 k or 2 k x 2 k		512 x 512 or 1 k x 1 k	
Quantum Efficiency (%)	>80		>50	
Dark Current (e^-/s)	<0.02	TBD	<1	
Read Noise (e^-), single-sample	<15		<15	
Well Capacity (e^-)	>60,000		>60,000	
Power Dissipation (mW)	tbd (minimize)		tbd (minimize)	

Development Plan

- Goals: Meet science goals by demonstrating
  - Improved sensitivity (lower i_{dark}, read noise)
  - Increased formats, w/ 512^2 up to $2k^2$ building blocks
- Approach: Plan technology development with
  - Open competition, peer review, science involvement
  - Present work (incl. extensions of SIRTF InSb and Si:As)
  - Planned work (incl. pursuing higher-T TIR options)
- Funding: Approx $12.5 M investment, over 6 yrs
- Deliverable: Flight prototype arrays (NIR, TIR) in ‘02

Building block array

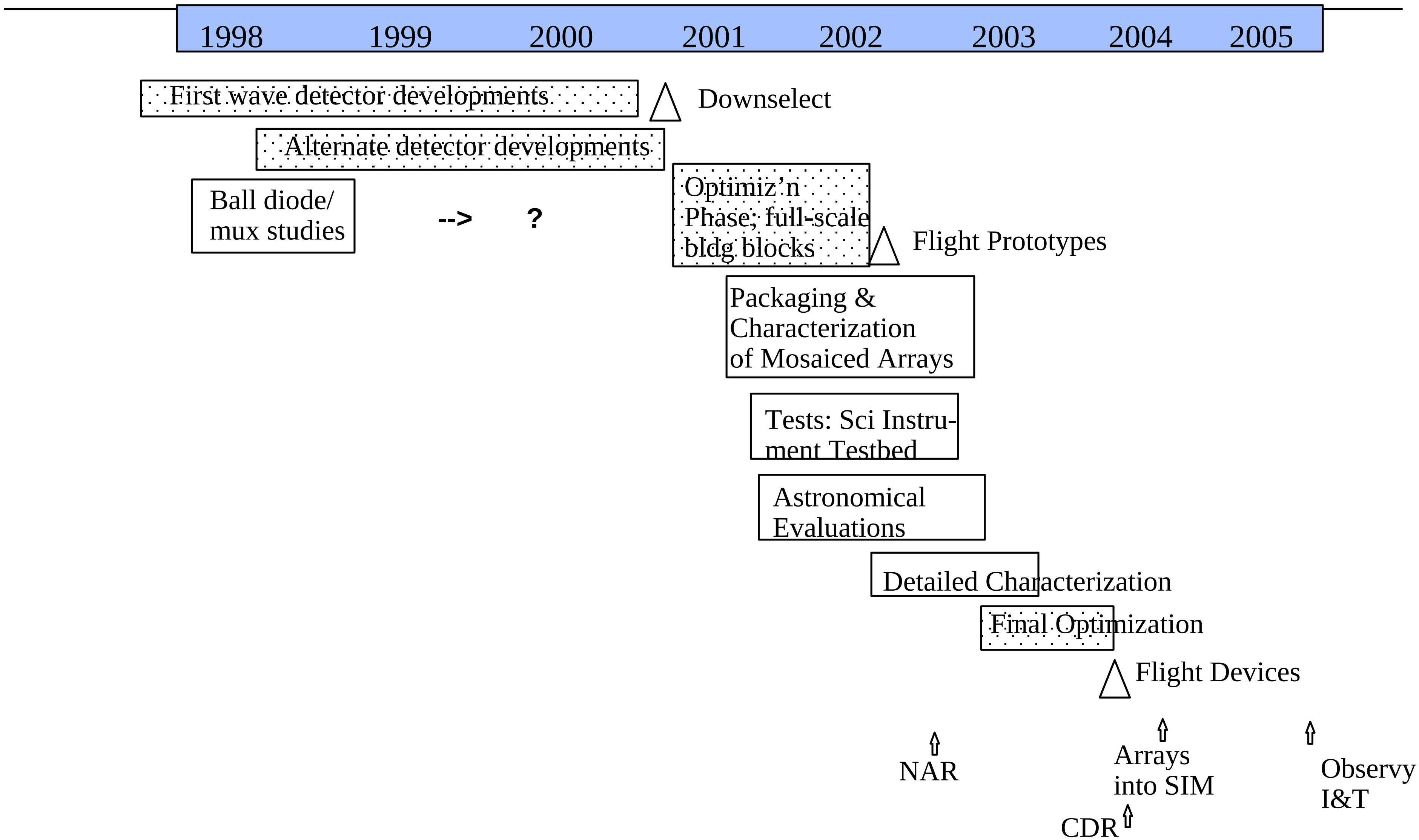




Flight prototype concept

NGST Detector Technology

Overall Development Plan



Near-IR Developments

	Title	Institutions	Comments
'first-wave'	1024 x 1024 InSb Arrays	University of Rochester teamed with Raytheon IRCoE (formerly SBRC)	Aims to develop 1024 x 1024 protoflight InSb arrays. Would meet NGST performance goals (3 e- read noise, 0.01 e-/s dark current, T = 30 K), in a layout which would be buttable to 4 k x 4 k formats. Incremental mux development: 256x256, leading to 412 x 512, leading to 1 k x 1 k. Shares a common readout approach with NGST Si:As task.
'second-wave'	1k x 1 k and 2 k x 2 k HgCdTe Arrays	University of Hawaii teamed with Rockwell Science Center	Will evaluate 1 k x 1 k HgCdTe arrays, and develop 2048 x 2048 HgCdTe arrays, of differing cutoff wavelengths, to fill NGST needs. Cutoffs in HgCdTe will be 5, 2.5, and 1.8 µm, with a limited amount of effort on Si p-i-n diodes. Readouts will be based on 18-µm pitch HAWAII-2, under development for ground-based applications. T = 30 K. Will measure and study dark current.
Industry-sponsored	Large Format Readouts / InSb Array Studies	Ball / Raytheon / American Microsystems, Inc.	Designed and produced 2 k x 2 k readouts, using 0.6 µm CMOS design rules, on 200 mm wafers. Room-temperature probing underway now, and cryogenic testing will start at Ball before the end of the year. 684 x 684 coupon to be used for cryo evaluation. Plans also include delivery of hybridized InSb arrays to Ball (planar and mesa structures) this fall, and commissioning of low-background array chamber.

Thermal-IR Developments

Spectral Range	Title	Institutions	Comments
‘first-wave’	Low Dark Current, High Quantum Efficiency 10 µm Arrays	University of Rochester teamed with Rockwell Science Center	Aims to develop 10 µm-cutoff HgCdTe arrays for 25 - 30 K operation. Near-term work focuses on designing & growing new [double layer planar heterojunction] detectors optimized for astronomical use, improving overall understanding of limiting mechanisms (esp. leakage), and characterizing available 10 µm devices. Pragmatic near-term goal is to demonstrate dark currents in the 100 to 1000 e-/s range.
‘first-wave’	Improved Si:As IBC Arrays	Ames Research Center teamed with Raytheon IRCoE & Cornell University	Aims to meet NGST performance goals in Si:As IBC arrays (28 µm cutoff), and to expand formats to 512 x 512 (buttable to 1 k x 1 k) and possibly 1 k x 1 k directly. Optimize Si:As detector design, based on SIRTF & new models, for even lower dark current. Work to achieve operating temperatures approaching 8 K, while maintaining low dark current. Shares a common readout approach with NGST InSb task.
‘second-wave’	Large-Format Si:Ga IBC Arrays	Boeing Research & Technology Center (formerly Rockwell)	Aims to develop a new epitaxial growth technology to produce gallium-doped silicon (18 µm cutoff) IBC detectors. Will aim to meet NGST sensitivity requirements. Will use 1 k x 1 k HAWAII multiplexer to demonstrate large formats. Calculate operating temperature about 4 kelvin higher than Si:As. Demonstrations performed with both Si:As samples and new Si:Ga devices.

InSb Development Strategy

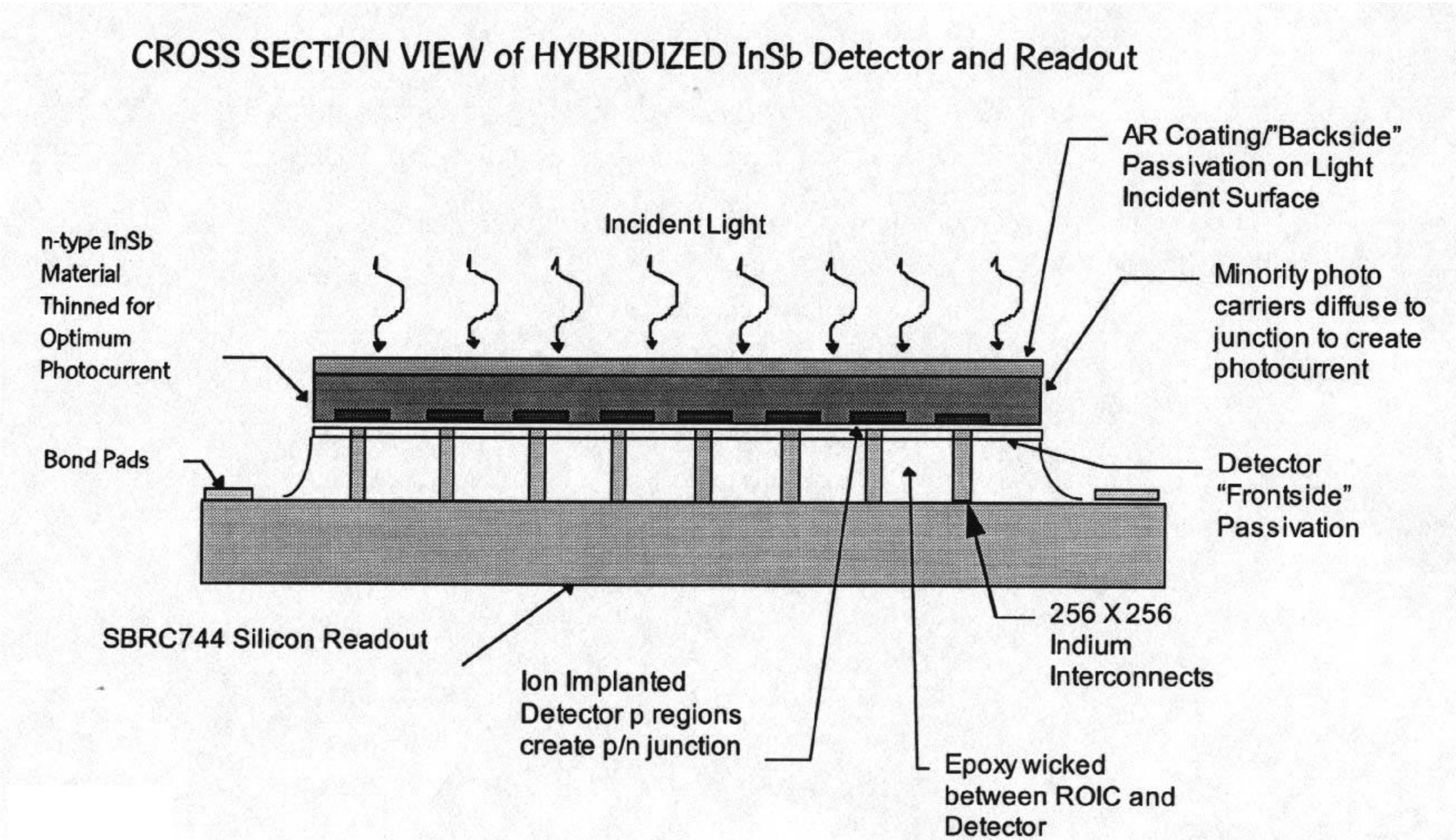
- **Improve InSb array performance (emphasize reduced read noise), and establish technology path (with adequate yield) to achieve buttable 4 k x 4 k arrays, with minimal gaps**

- **To improve read noise, three test readouts were designed, fabricated, & tested:**
  - **SBRC 187: same as CRC-744, with 1/2 and 1/2 on reset switch. Half has switch on drain side of unit cell; half has switch on source. (non-functional, due to design error)**
  - **SBRC 188: advanced architectures (CTIA; current mode amplifier). (successful.**
  - **SBRC 189: large format -- 412 x 512, using CRC-744 architecture. (successful -- yield ~15%)**

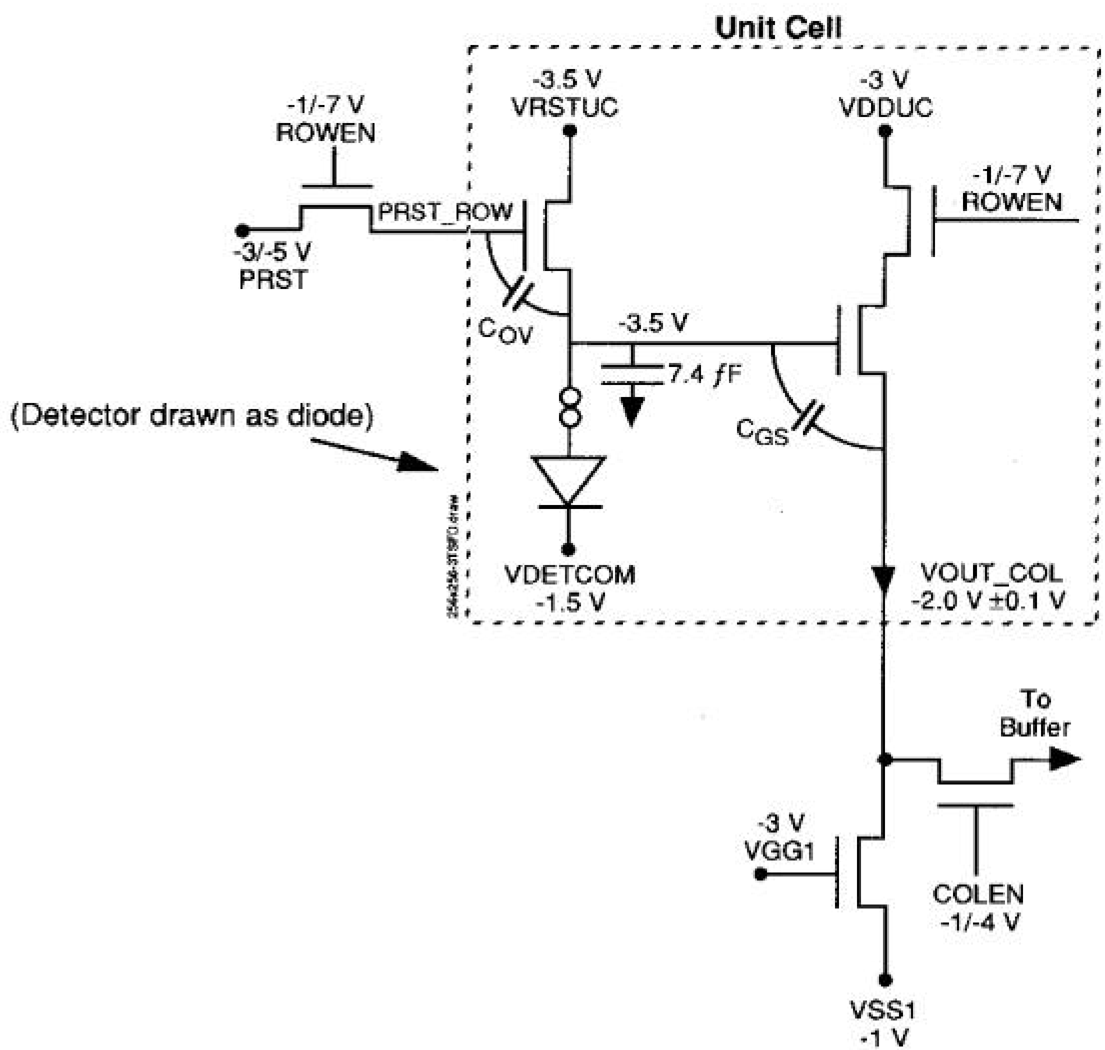
- **Carefully characterize voltage noise spectra of CRC-744 MOSFETs. Allowing refinements to theory.**

- **Stretch to 1 k x 1 k format. Design & process new advanced mux, at Orbit (emphasize 30 K operation)**

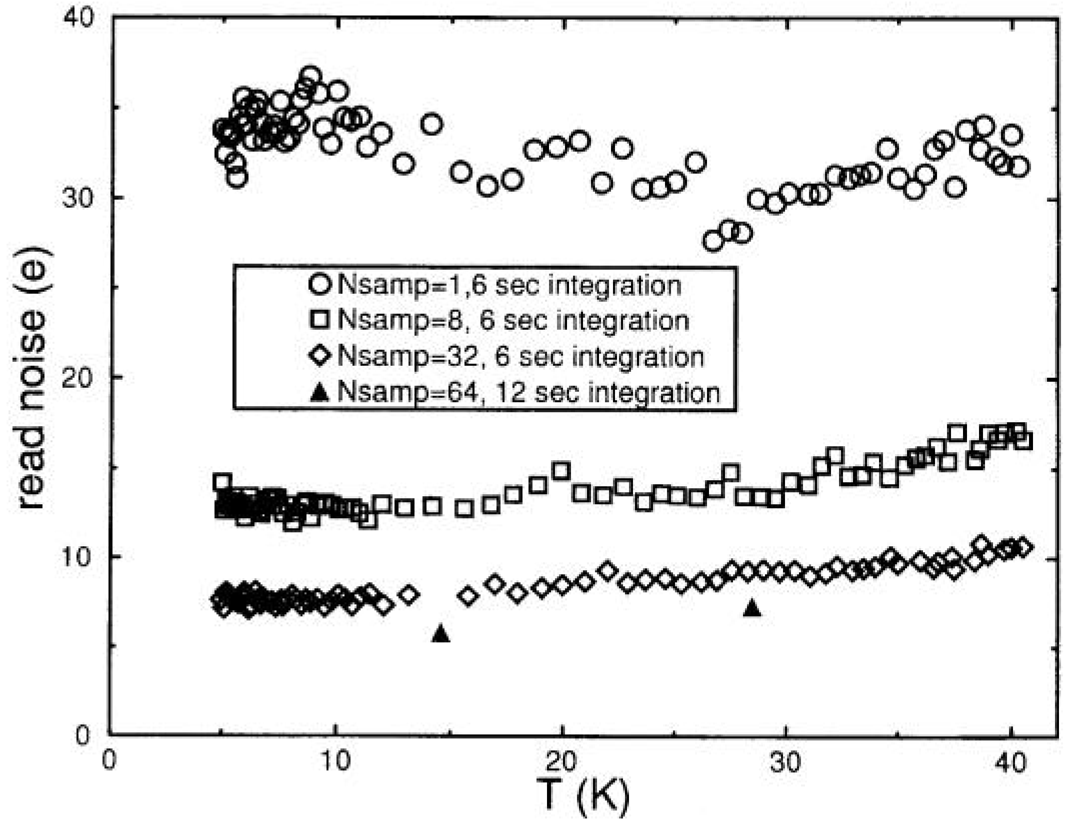
InSb Array Geometry



CRC-744 Cryogenic Readout Circuit



InSb Read Noise Data



Demonstrates read noise approaching NGST goals achieved via multiple sampling techniques.
SBRC cryoCMOS Si readouts.

5 µm HgCdTe Plans

Fabricate 2 k x 2 k muxes, augmenting HAWAII-2 foundry runs.

Produce & test 1.8, 2.5, and 5 µm cutoff HgCdTe arrays. MBE / double layer planar heterojunction on CdZnTe substrates

Initial hybrids: 256 x 256 detectors on sections of 2 k x 2 k readouts. Later, test full-scale arrays.

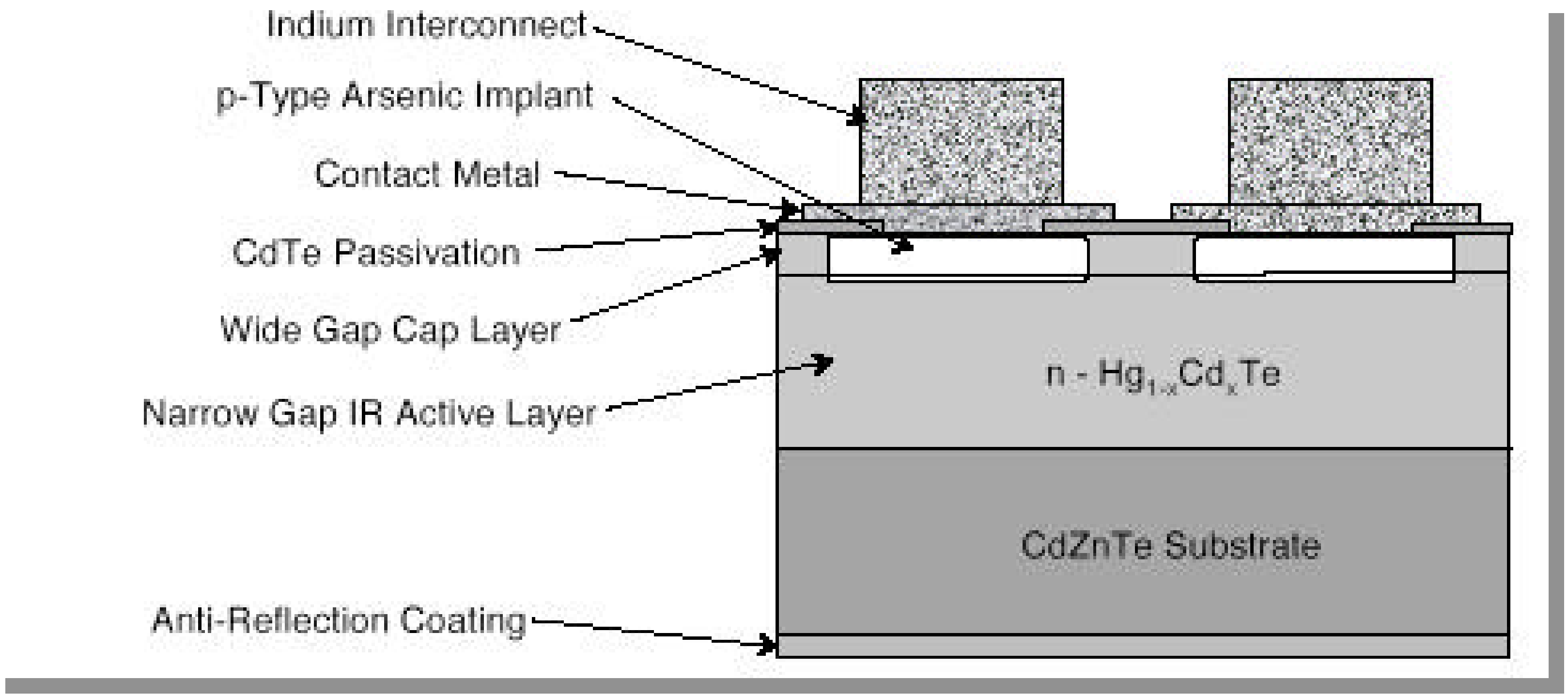
Test & carefully characterize.

Evaluate potential of silicon p-i-n diodes, mated to 2 k x 2 k muxes

Evaluate butted architectures (4 k x 4 k up to 8 k x 8 k)

Develop cost models for full arrays.

Rockwell HgCdTe Design



HgCdTe: Compression Layer

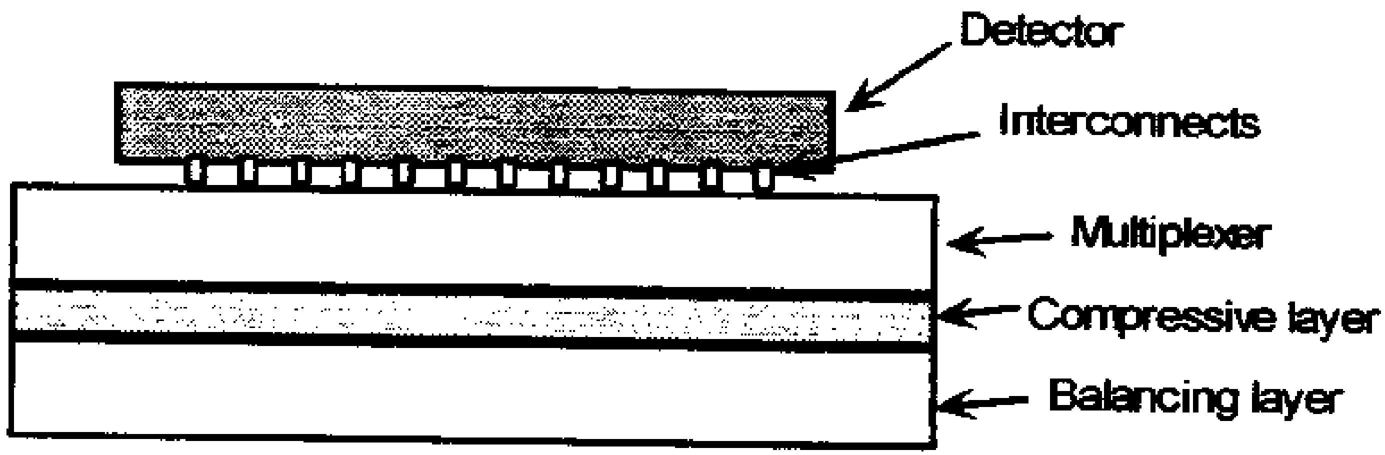
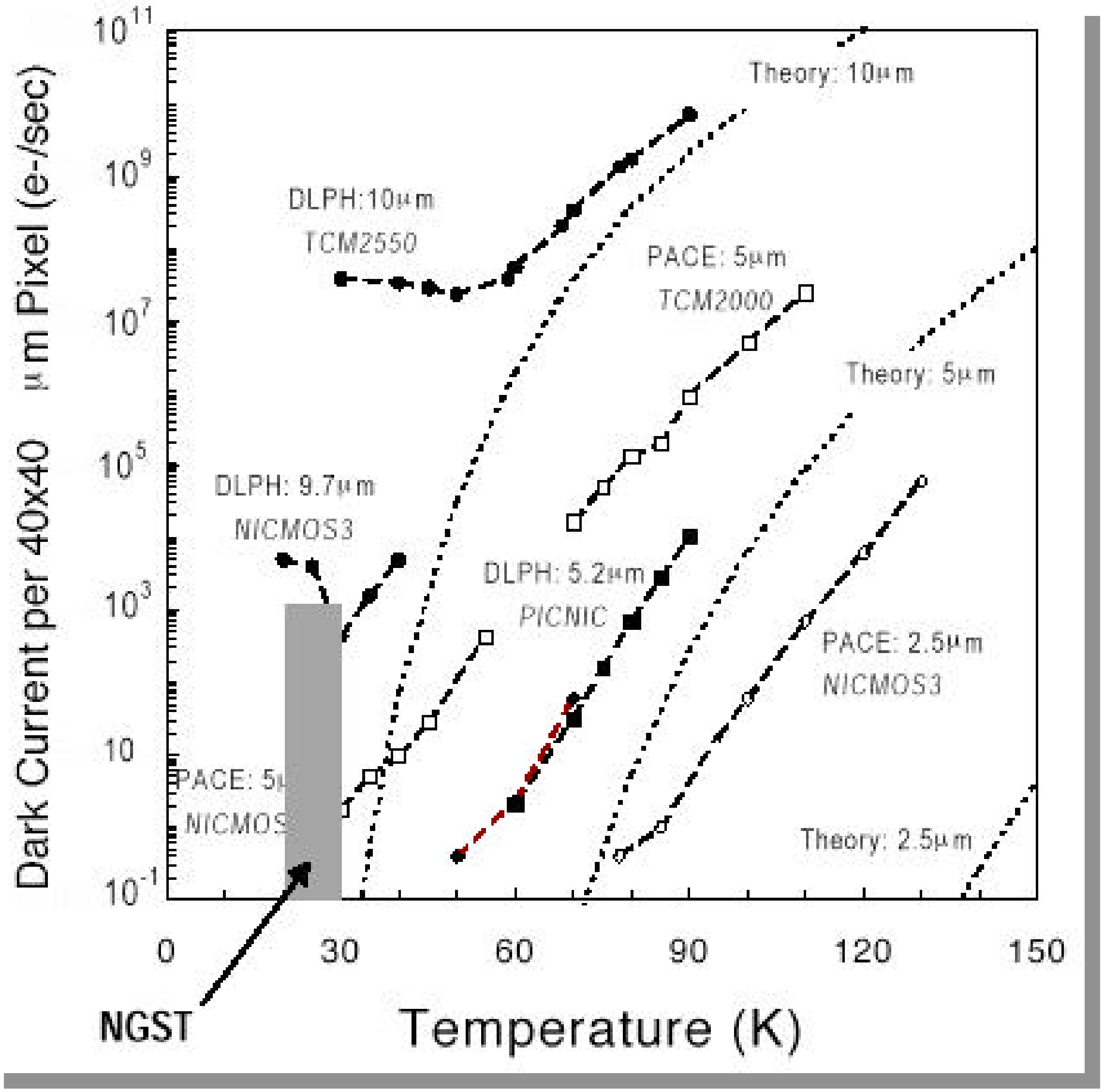
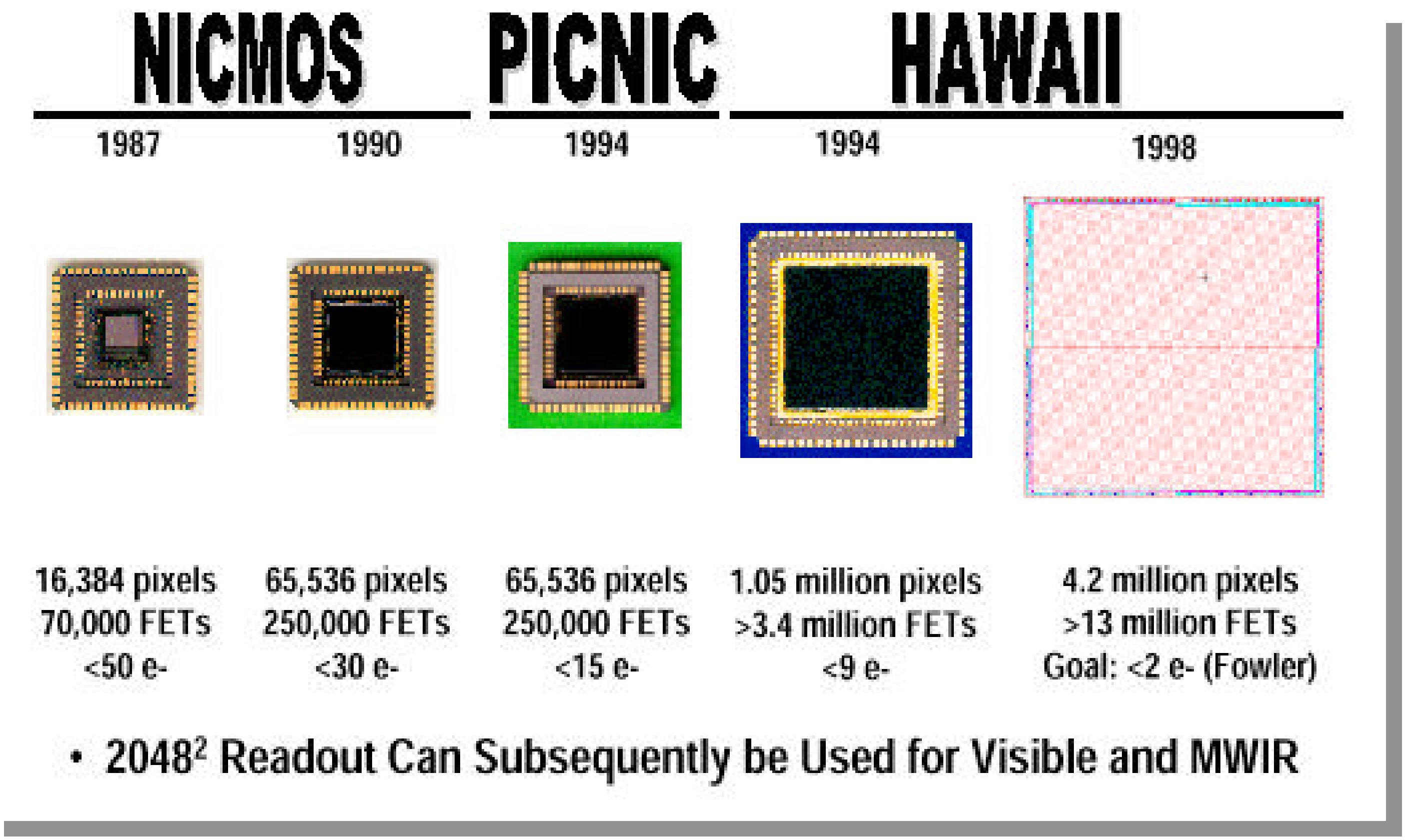


Figure 3.1: The BCS design compresses the mux to match the thermal contraction of the detector without bending the FPA.

NGST Detector Technology



NGST Detector Technology



10 μm HgCdTe Approach, Status

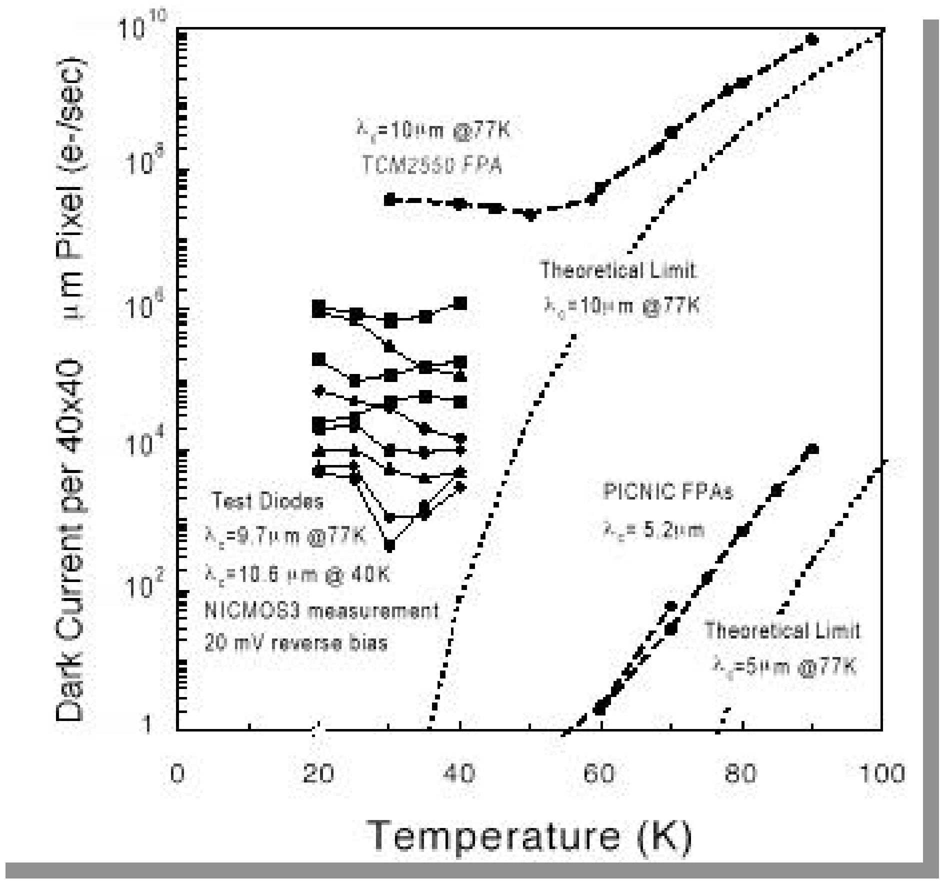
Utilize Double Layer Planar Heterojunction (DLPH) technology; aim for <100 e^-/s at ~30 K.

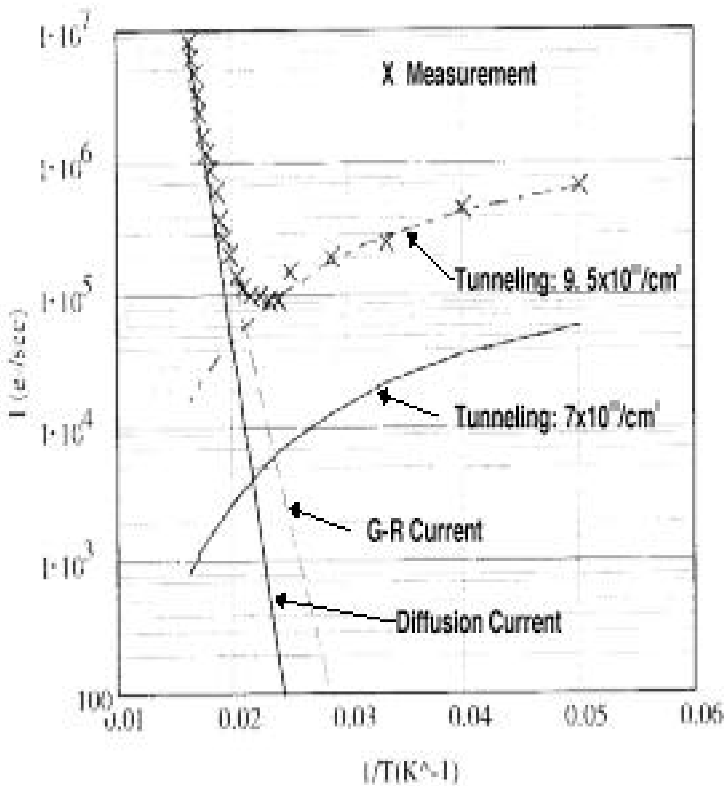
Single diodes (available) characterized. 256 x 256 test arrays recently received (with 7.1 & 9.1 μm cutoffs). Initial array leakage data show most pixels are <1000 e^-/s at 30 K.

New lots to be fabricated with advanced structure junctions, and lower doping levels (reduce trap-to-band contributions). Tunneling current model suggests potential 10x dark current reduction for modest detector base layer doping decrease. Passivation challenges

Need to expand data set, to include QE measurements, careful capacitance measurements, uniformity, etc.

10 µm HgCdTe Diode Tests





N_d=9.5x10^{14} for the λ_c=10.6 μm test detectors

Current vs T measured at 100mV reverse bias was fit to model including diffusion, G-R, and tunneling current.

Model predicts 10x reduction in minimum dark current for N_d=7x10^{14}.

Si:As Development Approach

Build upon SBRC SIRTF IBC technology base:

-optimized Si:As IBC structures

-low-noise, cryoCMOS epi readouts (CRC-744)

Utilize CRC-744 design, *closely coordinating with InSb effort*, to achieve

-quieter, lower-leakage readouts

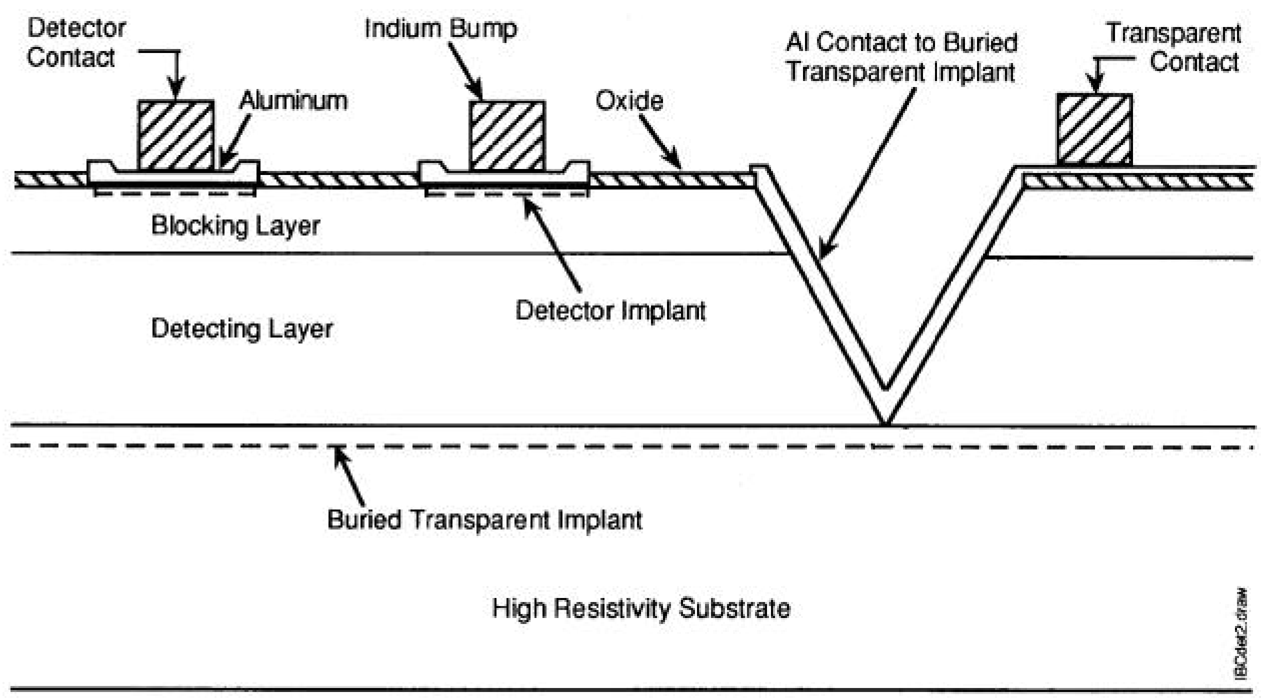
-larger formats (512 x 512, 1024 x 1024?)

Conduct detailed analytical and experimental studies, to better understand and reduce effects of limiting noise and dark current mechanisms

Produce and evaluate test structures. Complete multiple (3) iterations / lots, leading to optimized hybrid arrays

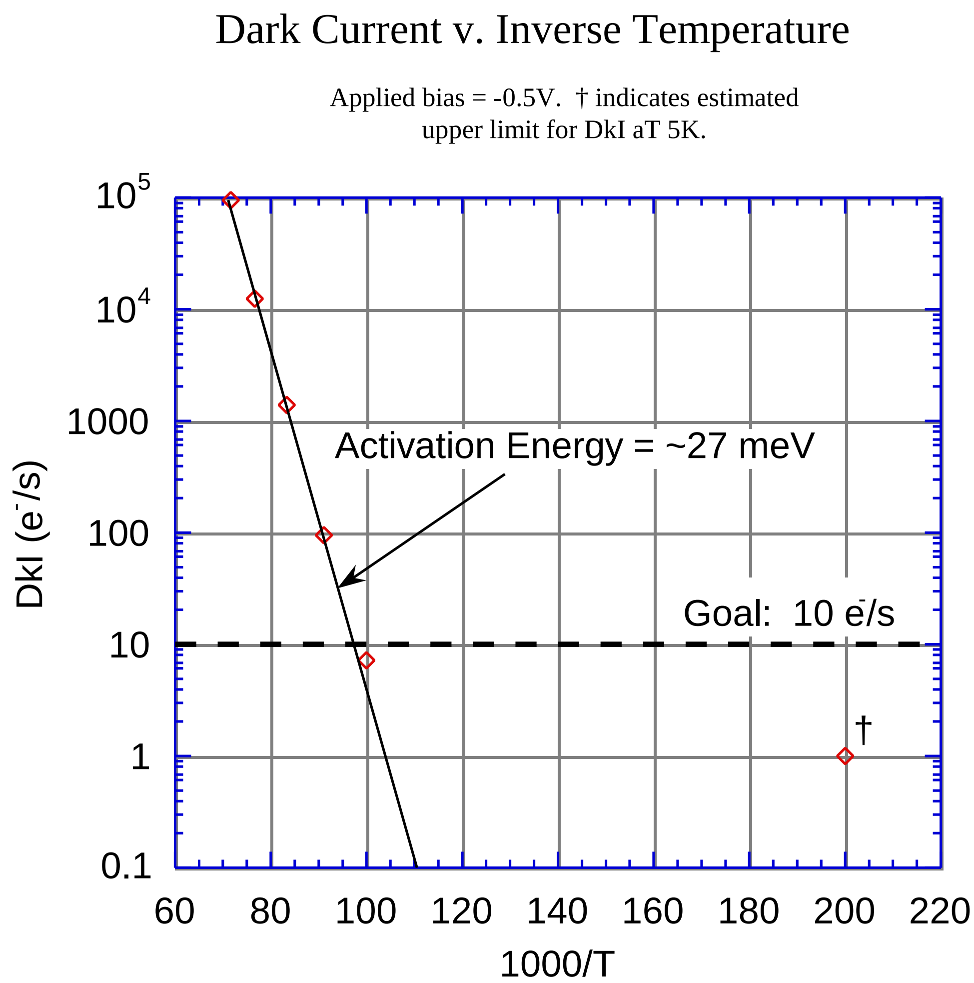
Improve the art & science of low-background radiometry -- to <0.05 ph/s

Hybrid IBC Array Structure



Si:As Dark Current vs. 1000/T

- Initial value of activation energy reasonable: 27 meV
- Initial dark current plot shows IRAC goal (10 e-/s) reachable at 10 K
- 5 K dark current un-measurably low at integration times as long as 300 s.



SIRTF /IRAC Si:As QE Data Encouraging

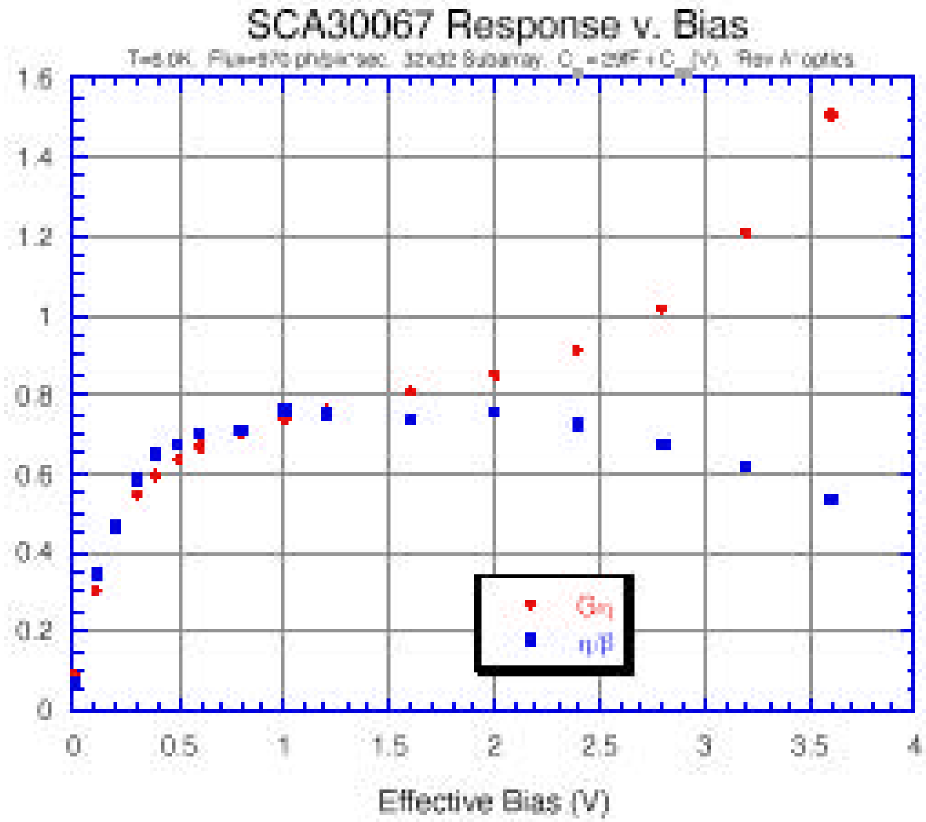
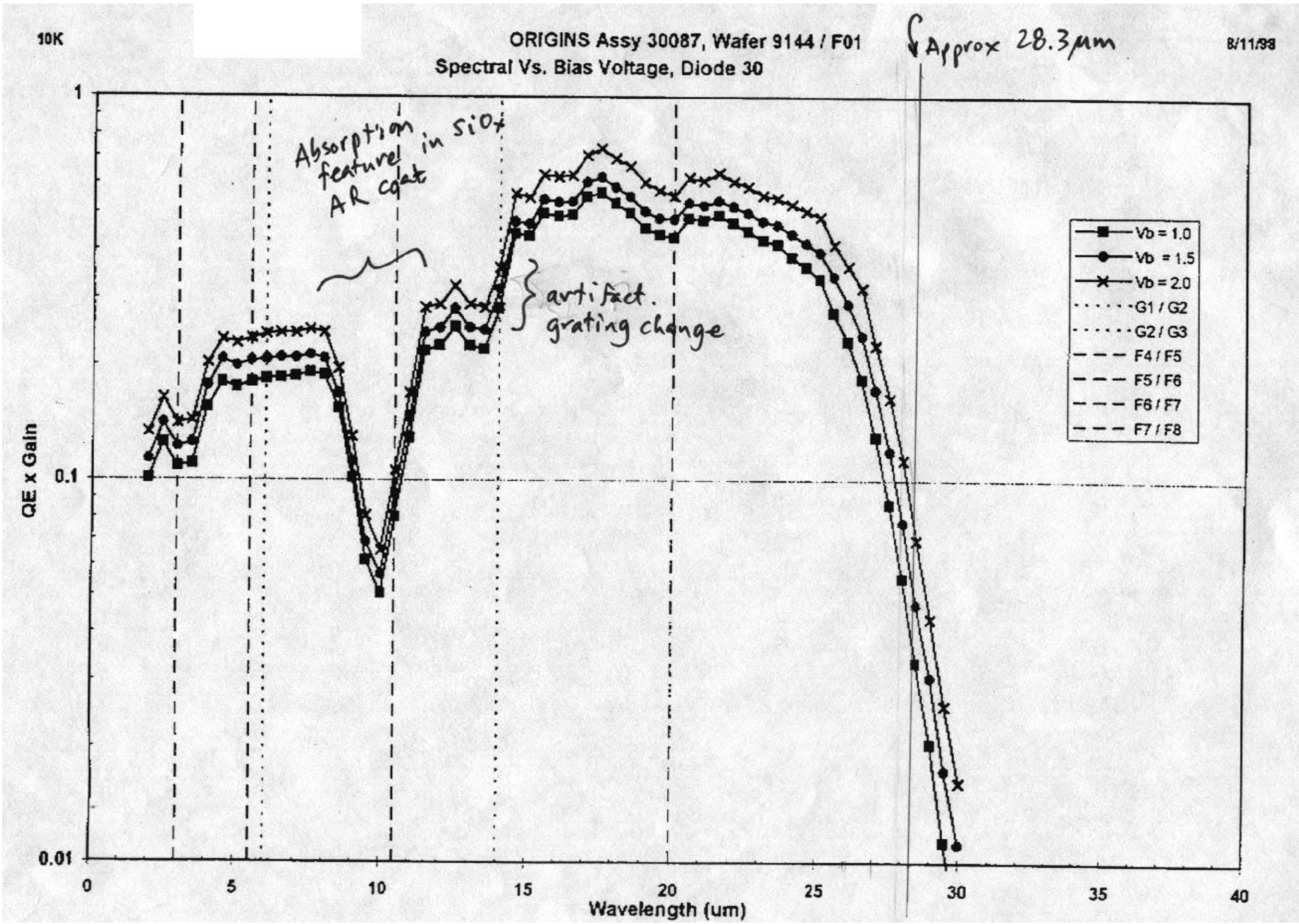


Figure 3. Responsive and detective quantum efficiency plotted as a function of effective bias. Effective bias as used here is VDET -2.6V.

NGST Detector Technology

Si:As IBC Spectral Response



Si:Ga IBC Development Plan

Develop gallium-doped silicon IBC arrays (18 μm cutoff; higher operating temperature). Collaborative effort with Lawrence Semiconductor Research Laboratory, using chemical vapor deposition. Leverage extensive experience in Si:As and Si:Sb developments for SIRTF and other applications.

Study (low-temperature) operation of IBC arrays on existing HAWAII mux (1 k x 1 k), with existing Si:As detectors. Identify performance attributes and problems, and design/fabricate advanced readouts. Push to reduce noise, power dissipation, via improved unit cell designs.

Characterize, and iterate, to move toward optimum designs.

Carry Si:As as backup.

Si:Ga Development Plan

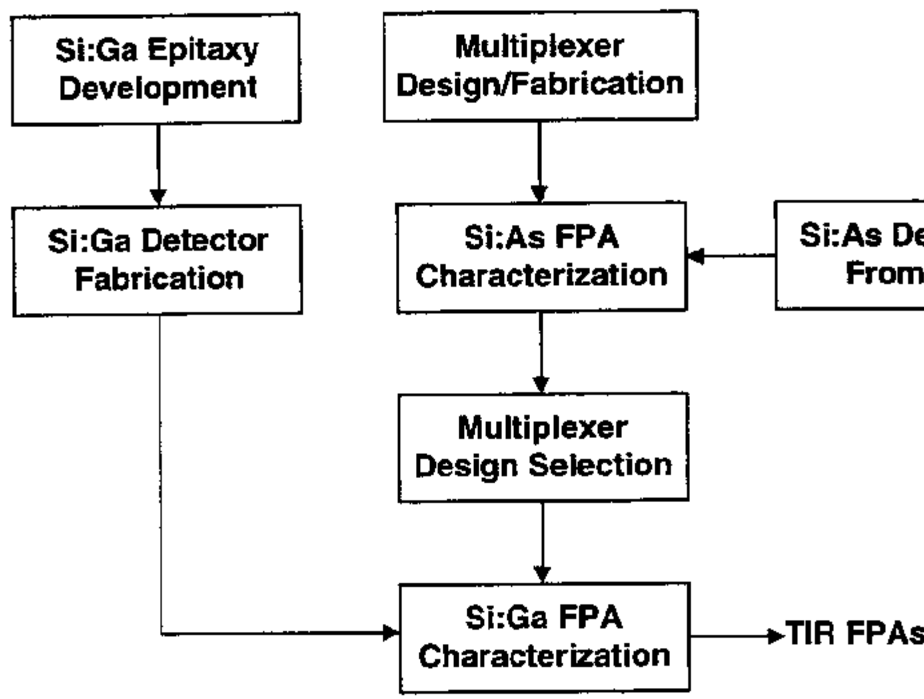


Figure 3. Block diagram of technical approach.

Si:Ga Predictions: T-dependence

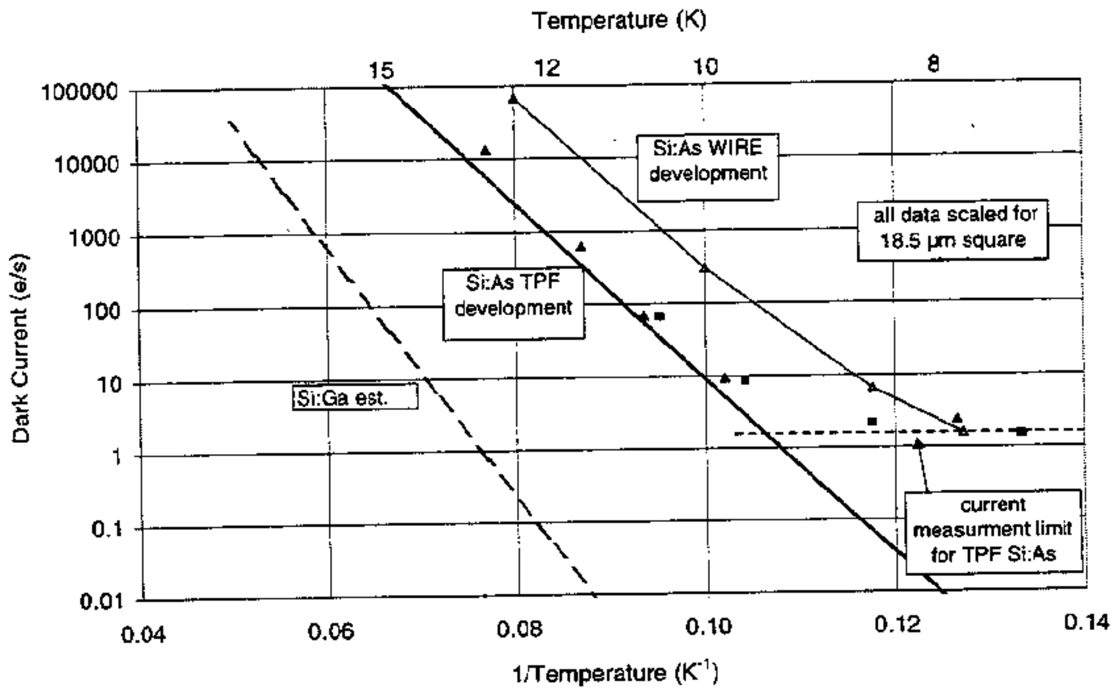


Figure 7. Comparison of dark current vs. operating temperature for Si:As and Si:Ga BIB detectors. The Si:Ga points are model predictions. The Si:As data are scaled from hybrid-level measurements using a detector of the same IR-active layer doping as used for the PEC measurements of Figure 4 through Figure 6. The pixel size assumed for the calculations was 18.5 µm. The deviation of the Si:As data from the model prediction at 7.9 K indicates the presence of measurement-system leakage current, optical background, or device current generated by non-thermal processes.

Additional Information

NGST Technology Challenge Review Proceedings

1998:
http://ngst.gsfc.nasa.gov/Hardware/meetings/techchalwest.html

1997:
http://ngst.gsfc.nasa.gov/Hardware/meetings/techchal1.html

Synopses of development progress